REMARKS/ARGUMENTS

1. Priority:

The applicant has claimed the benefit of foreign priority for this application. However, the applicant does not understand what the Examiner wrote in the Office action regarding "declaration of an interference". If this application is involved in an interference, the applicant requests the Examiner to provide more details.

2. Rejections of claims 1, 2, 5-12 and 15 under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,140,224) in view of Cole et al. (US 5,338,975) and Kern (Handbook of Semiconductor Wafer Cleaning Technology – Science, Technology, and Applications; 1993; William Andrew Publshing/Noyes.) and Pintchovski et al. (US 4,822,753):

Claim 1 has been amended to overcome the rejection under 35 U.S.C 103(a) as set forth in the above detailed Office action. Specifically, the limitations " forming a **Ti/TiN film**, functioning as the barrier layer, onto the **cobalt silicide**" and "performing a wet etching process to remove the barrier layer, the wet etching process being implemented with an acid solution comprising phosphoric acid (H_3PO_4), nitric acid (HNO_3), acetic acid (CH_3COOH), and water (H_2O), wherein the ratio of phosphoric acid, nitric acid, acetic acid, and water in the acid solution is between **(38-41):(1-1.5):(1.8-2.1):(2.8-3.2)**" have been added to claim 1. These limitations find support in the specification in paragraph [0018] and in original claim 3 for instance, and no new matter is entered.

In the cited arts, Lin discloses a method of forming a tungsten plug including steps of forming barrier layer, Cole teaches forming a high density interconnect structure in which the spacer structure and the adhesive layers can be removed and reworked, Kern teaches defect detection and brush scrubbing technique, and Pintochovski teaches a method of a contact which includes etching to remove the barrier layer.

The Examiner interprets the spacer structure and the adhesive layer in Cole's disclosure as a barrier layer, however, the barrier layer of claim 1 is Ti/TiN film, and none of these layers disclosed in Cole's teaching are made of Ti/TiN. In addition, Cole's high density interconnect structure is fabricated after chips are already made. That means Cole's teaching is implemented in the back-end process (e.g. package process), and the spacer structure or adhesive layer to be reworked is used as support means or adhesion means instead of an electrical component. On the other hand, the method of the present application is used to reform Ti/TiN film, which is a front-end process and functions electrically. Therefore, the applicant believes that no prior art has disclosed a rework method in the field of Ti/TiN barrier layer and the reworkability of spacer structure or adhesive layer is distinct from claim 1. It would not have been obvious to one ordinary skill in the art at the time of invention was made to combine the cited arts to obtain the method of the present application.

In addition, the Examiner cited Yamazaki (US 6,613,614) and reject claims 3-4. The applicant thinks it is improper to use Yamazaki's teaching to reject claims 3-4. Claims 3-4 discloses using an acid solution comprising phosphoric acid (H_3PO_4), nitric acid (HNO_3), acetic acid (CH_3COOH), and water (H_2O) of a ratio of (38-41):(1-1.5):(1.8-2.1):(2.8-3.2). In the

amended claim 1, this limitation has been added, so has the limitation "the **Ti/TiN film** is formed on the **cobalt silicide**". The acid solution of the present application is used to remove the Ti/TiN film, and the ratio is critical to the etching selectivity between Ti/TiN and cobalt silicide. On the other hand, the acid solution containing chromium proposed by yamazaki is used to etch **alumina film** without etching **aluminum film** (col 2, line 64 to col. 3, line 5). Since the ratio is crucial to the etching selectivity between Ti/TiN and cobalt silicide, and Yamazaki fails to teach his acid solution can be used to etch Ti/TiN without cobalt silicide, the quantity difference between the claimed ratio and Yamazaki's ratio should not and cannot be ignored. Therefore, the amended claim 1 should be allowed. Claims 2 and 5-6 are dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claims 1-2 and 5-6 is politely request.

Claim 7 has been amended to overcome the rejection under 35 U.S.C 103(a) as set forth in the above detailed Office action. Specifically, the limitation "forming a **Ti/TiN film** onto the conducting layer" has been added to claim 7. This limitation finds support in original claim 8 for instance, and no new matter is entered.

The Examiner interprets the spacer structure and the adhesive layer in Cole's disclosure as a barrier layer, however, claim 7 discloses forming a Ti/TiN film, and none of these layers in Cole's teaching are made of Ti/TiN. In addition, Cole's high density interconnect structure is fabricated after chips are already made. That means Cole's teaching is implemented in the back-end process (e.g. package process), and the spacer structure or adhesive layer to be reworked is used as support means or adhesion means

instead of an electrical component. On the other hand, the method of the present application is used to reform Ti/TiN film, which is a front-end process and functions electrically. Therefore, the applicant believes that no prior art has disclosed a rework method in the field of Ti/TiN film and the reworkability of spacer structure or adhesive layer is distinct from claim 7. It would not have been obvious to one ordinary skill in the art at the time of invention was made to combine the cited arts to obtain the method of the present application. Therefore, the amended claim 7 should be allowed. Claims 9-12 and 15 are dependent on claim 7, and should be allowed if claim 7 is found allowable. Claim 8 has been cancelled. Reconsideration of claims 7, 9-12 and 15 is politely request.

2. Rejections of claims 3, 4 and 13-14 under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,140,224) in view of Cole et al. (US 5,338,975) and Kern (Handbook of Semiconductor Wafer Cleaning Technology – Science, Technology, and Applications; 1993; William Andrew Publshing/Noyes.) and Pintchovski et al. (US 4,822,753) in further view of Yamazaki et al. (US 6,613,614):

Claims 3-4 have been cancelled. Claims 13-14 are dependent on claim 7, and should be allowed if claim 7 is found allowable. Reconsideration of claims 13-14 is therefore politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: November 11, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)